APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/018,658	12/21/2001	Kunijuki Kajita	L9289.01227	2181

24257 7590 04/19/2005		EXAMINER	
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ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 04/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
  after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
  earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _18 February 2005_.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is
closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _34-51_ is/are pending in the application.

　　4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _34-51_ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

　　Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

　　Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

　　a)☐ All ・ b)☐ Some * c)☐ None of:

　　　　1.☐ Certified copies of the priority documents have been received.

　　　　2.☐ Certified copies of the priority documents have been received in Application No. _____.

　　　　3.☐ Copies of the certified copies of the priority documents have been received in this National Stage
application from the International Bureau (PCT Rule 17.2(a)).

　　* See the attached detailed Office action for a list of the certified copies not received.

DETAILED ACTION

Response to Amendment

Applicant's arguments/amendments with respect to amended claims 34-36 and 46-48 and previously presented claims 37-45 and 49-51 filed February 18, 2005 have been fully considered but are not persuasive.

Applicant contends, "...Kato (prior art of record) discloses Figure 2...adding dummy data to make the packets of the same length, and there after attaching the CRC to the packets...thus the CRC are added <u>after</u> the dummy data is inserted...in the present claims the CRC bits are added to the transport blocks prior to the addition of the at least one predetermined bit to the beginning...the purpose of adding at least one predetermine bit...is so that the CRC bit will be the last bit thereof. The Examiner respectfully disagrees. Kato clearly teaches in Figure 5d, the CRC to be the last bit thereof. The order of operations does not necessarily render the claims patentably distinct over the prior art of record. *In Re Dailey, 149 USPQ 47 (CCPA 1976)*:

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies are not recited in the rejected claim(s). For example, Applicant contends, "Kato doe not teach operation of dividing the transport data into the plural transport blocks. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

The Examiner disagrees with the Applicant and maintains rejections with amended claims 34-

36 and 46-48 and previously presented claims 37-45 and 49-51. All arguments have been

considered. It is the Examiner's conclusion that amended claims 34-36 and 46-48 and

previously presented claims 37-45 and 49-51 are not patentably distinct or non-obvious over the

prior art of record.

Claim Rejections - 35 USC § 103

The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966),

that are applied for establishing a background for determining obviousness under 35

U.S.C. 103(a) are summarized as follows:

1.   Determining the scope and contents of the prior art.
2.   Ascertaining the differences between the prior art and the claims at issue.
3.   Resolving the level of ordinary skill in the pertinent art.
4.   Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 34-51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kato (USPN

5844918). Prior OA:

As per claims 34-36 and 46-48, Kato substantially teaches (title and abstract) an error

correcting code including basic data and a BCH-based parity code appended thereto is divided

into smaller packets. An error detecting code is appended to each of the thus-divided packets, so

that transmission basic data is formed. When the transmission basic data is received, the basic

data and a BCH-based parity code are derived from the transmission basic data. Error correcting

is carried out with respect to the overall transmission basic data. An error detecting operation is

carried out with respect to each packet using the error detecting code. If a packet is found to
contain errors, a request for retransmission of that packet will be sent to the sending side. Kato
teaches (col. 16, lines 39-67) a digital transmission method for sending a digital signal
comprising: a division step of dividing an error correcting code which includes basic data and a
parity code, into smaller data segments; an error detecting code addition step of appending an
error detecting code to each of the data segments divided in the division step; a transmission step
of sending the data segments complete with the error detecting code on a packet-by-packet basis;
and a retransmission step of retransmitting a requested data packet in response to a
retransmission request of the data packet from a receiving side. This procedure in shown by
example in Figure 5, wherein the input terminal 10 of the data transmitter A receives the basic
transmission data AD (see FIG. 5A), and the received basic transmission data is sent to the
packet assembly circuit 12. The basic transmission data AD has already been changed to a BCH
code by addition of a BCH-based parity code to the basic data BD as a result of the FEC
operation. The basic transmission data AD is divided into data segments by the segmentation
circuit 14 of the packet assembly circuit 12 so that they can be assembled into packets, as shown
in FIG. 5b. The error detecting code addition circuit 16 appends the CRC code to each data
segment, as shown in FIG. 5c. The header addition circuit 20 appends a packet header to the
data segment complete with the error detecting code, whereby a transmission data packet is
assembled, as shown in FIG. 5d. The thus-assembled transmission data packet is stored in the
data memory 22 and sent to the data receiver B via the transmit/receive circuit 24.

Kato does not explicitly teach a concatenating unit that concatenates each of the data
blocks having the CRC as stated in the present application.

However, the Examiner would like to point out that Kato teaches in Figure 5B to divide

the basic data, which is analogous to transport blocks of the present application. CRC is then

appended to each of the data blocks. Although Kato does not explicitly teach to concatenate all

of the CRC data blocks, he does show a data memory (Figure 4, Reference #44), which is used to

store the transmitted packets in case of a request for retransmission. Therefore, it would have

been obvious to one of ordinary skill in the art at the time the invention was made to add a

concatenating unit to concatenate the CRC data blocks. This modification would have been

obvious to one of ordinary skill in the art because one of ordinary skill in the art would have

recognized that by using a concatenating unit to concatenate the CRC data blocks would improve

on packet synchronization during transmission.

As per claims 37-39 and 49-51, Kato substantially teaches, in view of above rejections,

(Figure 5 and col. 9, lines 10-37) the input terminal 10 of the data transmitter A receives the

basic transmission data AD (see FIG. 5A), and the thus-received basic transmission data is sent

to the packet assembly circuit 12. The basic transmission data AD has already been changed to a

BCH code by addition of a BCH-based parity code to the basic data BD as a result of the FEC

operation. The basic transmission data AD is divided into data segments by the segmentation

circuit 14 of the packet assembly circuit 12 so that they can be assembled into packets, as shown

in FIG. 5b. The error detecting code addition circuit 16 appends the CRC code to each data

segment, as shown in FIG. 5c. The header addition circuit 20 appends a packet header to the

data segment complete with the error detecting code, whereby a transmission data packet is

assembled, as shown in FIG. 5d. The Examiner would like to point out that at least one of the

segmented data blocks in Figure 5D has less data than the other data blocks. Subsequently, the

assembled transmission data packet is stored in the data memory 22 and sent to the data receiver

B via the transmit/receive circuit 24. Kato also teaches (col. 16, lines 53-68) a digital

transmission method for sending a digital signal, comprising: a division step of dividing an error

correcting code which includes basic data and a parity code, into smaller data segments; an error

detecting code addition step of appending an error detecting code to each of the data segments

divided in the division step; a transmission step of sending the data segments complete with the

error detecting code on a packet-by-packet basis; and a retransmission step of retransmitting a

requested data packet in response to a retransmission request of the data packet from a receiving

side.

As per claims 40-45, Kato substantially teaches, in view of above rejections, (Figure 4)

the system and method digital data transmission to be for a communications system which

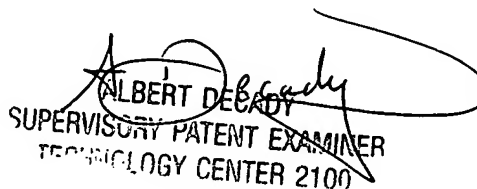obviously encompasses a mobile station and a base station.

Conclusion

Any inquiries concerning this communication should be directed to the examiner,

Mujtaba Chaudry who may be reached at 571-272-3817. The examiner may normally be reached

Mon – Thur 6:30 am to 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, please contact the

examiner's supervisor, Albert DeCady at 571-272-3819.

Mujtaba Chaudry
Art Unit 2133
April 5, 2005

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